CLAIMS

1. A process for manufacturing a byte selection transistor for a matrix of non volatile memory cells organised in rows and columns integrated on a semiconductor substrate, each memory cell comprising a floating gate transistor and a selection transistor, the process providing the following steps:

defining on a semiconductor substrate one or more active areas for said byte selection transistor, for said floating gate transistor and for said selection transistor, the active areas having portions of an insulating layer adjacent thereto;

depositing a multilayer structure comprising at least a gate oxide layer, a first polysilicon layer, a dielectric layer and a second polysilicon layer;

removing through a photolithographic technique said multilayer structure to form at least two bands, the first band being effective to define the gate regions of said byte selection transistor and of said selection transistor, the second band being effective to define the gate region of said floating gate transistor, a portion of said first band further extending on the portion of insulating layer which is adjacent to said byte selection transistor,

forming an opening in said portion to expose said first polysilicon layer,

forming a conductive layer in said opening to put said first polysilicon layer in electrical contact with said second polysilicon layer.

2. The process for manufacturing a byte selection transistor according to claim 1, characterized in that said portion that extends over the insulating layer has a greater width than the width of the gate regions of single transistors.

3. The process for manufacturing a byte selection transistor according to claim 1, characterised in that said conductive layer is a polysilicon layer.

4. The process for manufacturing a byte selection transistor according to claim 1, characterised in that said conductive layer is a metallization layer.

5. The process for manufacturing a byte selection transistor according to claim 1, further including:

a silicide layer on said second polysilicon layer and on the portion of said first polysilicon layer exposed through said opening.

6. A circuit structure comprising a matrix of non volatile memory cells organised in rows and columns integrated on a semiconductor substrate, the substrate having thereon circuitry comprising high and low voltage transistors, each memory cell comprising a floating gate transistor and a selection transistor, said rows being interrupted by at least a couple of byte selection transistors, said transistors being manufactured in respective active areas delimited by portions of an insulating layer, said circuit structure having a first and a second multilayer band formed on said semiconductor substrate, each band having a first gate oxide layer, a first polysilicon layer, a second dielectric layer and a second polysilicon layer, said first band defining the gate regions of said byte selection transistor and of said selection transistor in correspondence with said respective active areas and having a portion extending on a portion of the insulating layer adjacent to said byte selection transistor, said second band defining the gate regions of said floating gate transistor, wherein said portion is provided with an opening, formed in said second dielectric layer and in said second polysilicon layer, filled at least partially by a conductive layer.

7. The circuit structure according to claim 6, characterized in that said portion has a greater width at the location of said opening than the width at the location of said active areas.

8. The circuit structure according to claim 6, characterised in that said conductive layer is a polysilicon layer.

9. The circuit structure according to claim 6, characterised in that said conductive layer is a metallization layer.